Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): ~~A low power a reconfigurable processor core,~~ An apparatus comprising:

an integrated circuit comprising:

a plurality of processor units, each unit having a clock input ~~that controls~~ to control ~~the~~ performance of the unit; and

a controller having a plurality of clock outputs each coupled to ~~the~~ a respective clock input of ~~each~~ one of the processor units ~~unit~~, the controller to vary a ~~varying the~~ clock frequency of each processor unit ~~to optimize power consumption and processing power for a task~~.

Claim 2 (currently amended): The ~~processor core~~ apparatus of claim 1, wherein at least one of the processor units comprises a digital signal processor (DSP).

Claim 3 (currently amended): The ~~processor core~~ apparatus of claim 1, wherein at least one of the processor units comprises a reduced instruction set computer (RISC) processor.

Claim 4 (currently amended): The ~~processor core~~ apparatus of claim 1, wherein each processor unit is dynamically managed on a per-task basis.

Claim 5 (currently amended): The ~~processor core~~ apparatus of claim 1, wherein each unit is clocked at the lowest rate possible to reduce peak power dissipation, reduce average power dissipation, or minimize buffer memory size and power.

Claim 6 (currently amended): The ~~processor core~~ apparatus of claim 1, wherein the controller ~~generates~~ to generate a plurality of clock signals, each independently rate controlled to each processor unit.

Claim 7 (currently amended): The ~~processor core~~ apparatus of claim 6, wherein the plurality of ~~clocks is~~ clock signals are derived from a master clock.

Claim 8 (currently amended): The ~~processor core~~ apparatus of claim [[1]] 6, wherein the plurality of ~~clocks~~ clock signals comprise gated versions of a master clock.

Claim 9 (currently amended): The ~~processor core~~ apparatus of claim 1, wherein the controller ~~changes~~ to change the clock rate of each processor unit independently of the remaining processor ~~unit~~ units.

Claims 10-18 (cancel)

Claim 19 (currently amended): The ~~processor core~~ apparatus of claim 1, further comprising a buffer coupled between two of the plurality of processor units.

Claim 20 (currently amended): The ~~processor core~~ apparatus of claim 19, wherein the buffer is a first-in-first-out (FIFO) buffer.

Claim 21 (new): The apparatus of claim 1, wherein the integrated circuit further comprises a first wireless transceiver coupled to the plurality of processor units.

Claim 22 (new): The apparatus of claim 21, wherein the integrated circuit further comprises a second wireless transceiver coupled to the plurality of processor units.

Claim 23 (new): The apparatus of claim 21, wherein the plurality of processor units and the first wireless transceiver are on a single substrate.

Claim 24 (new): A system comprising:

a display; and

an integrated circuit on a single substrate coupled to the display, the integrated circuit comprising:

a plurality of processor units, each unit having a clock input to control performance of the unit;

a controller having a plurality of clock outputs each coupled to a respective clock input of one of the plurality of processor units, the controller to vary a clock frequency of each processor unit; and

a first wireless transceiver coupled to the plurality of processor units.

Claim 25 (new): The system of claim 24, wherein the integrated circuit further comprises a second wireless transceiver coupled to the plurality of processor units.

Claim 26 (new): The system of claim 23, further comprising a buffer coupled between a first one and a second one of the plurality of processor units.

Claim 27 (new): A method comprising:

generating a plurality of clock signals on an integrated circuit, each of the plurality of clock signals variable under control of a controller on the integrated circuit; and

providing each of the plurality of clock signals to a corresponding one of a plurality of processor units on the integrated circuit.

Claim 28 (new): The method of claim 27, further comprising varying at least one of the plurality of clock signals using the controller.

Claim 29 (new): The method of claim 27, further comprising dynamically managing the clock signal for a corresponding processor unit on a per-task basis.

Claim 30 (new): The method of claim 27, further comprising independently rate controlling each of the plurality of clock signals.

Claim 31 (new): The method of claim 27, further comprising providing a clock signal controlled by the controller to a wireless transceiver on the integrated circuit.